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Reconfigurable Ion Gating of 2H-$MoTe_2$ Field-Effect Transistors Using Poly(ethylene oxide)-$CsClO_4$ Solid Polymer Electrolyte

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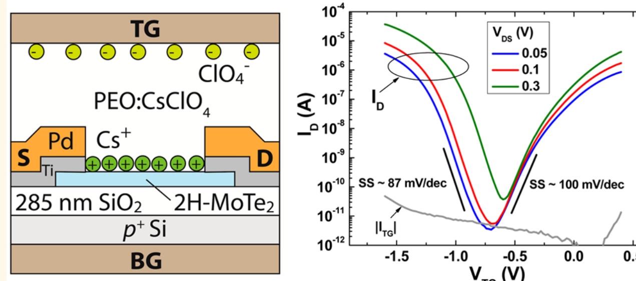
ABSTRACT Transition metal dichalcogenides are relevant for electronic devices owing to their sizable band gaps and absence of dangling bonds on their surfaces. For device development, a controllable method for doping these materials is essential. In this paper, we demonstrate an electrostatic gating method using a solid polymer electrolyte, poly(ethylene oxide) and $CsClO_4$, on exfoliated, multilayer 2H-$MoTe_2$. The electrolyte enables the device to be efficiently reconfigured between *n*- and *p*-channel operation with ON/OFF ratios of approximately 5 decades. Sheet carrier densities as high as 1.6×10^{13} cm^{-2} can be achieved because of a large electric double layer capacitance (measured as 4 μF/cm^2). Further, we show that an in-plane electric field can be used to establish a cation/anion transition region between source and drain, forming a p–n junction in the 2H-$MoTe_2$ channel. This junction is locked in place by decreasing the temperature of the device below the glass transition temperature of the electrolyte. The ideality factor of the p–n junction is 2.3, suggesting that the junction is recombination dominated.



KEYWORDS: field effect transistor · electrostatic gating · p–n junction · transition metal dichalcogenides · molybdenum ditelluride · polymer electrolyte · poly(ethylene oxide)

Transition metal dichalcogenides (TMDs) are two-dimensional (2-D), atomically thin crystals of broad interest for use in field-effect transistors (FETs),[1−4] tunnel field-effect transistors (TFETs),[2,5−7] and optoelectronic devices.[8−11] There are a growing number of experimental demonstrations of TMD FETs in materials such as MoS_2,[4,12−16] WSe_2,[17−22] and $MoTe_2$.[23−27] For TFETs, TMDs with a narrow band gap such as WSe_2 and $MoTe_2$, are needed to increase current drive.[5,7] Experimental demonstrations of back-gated TMD FETs are now being reported across a wide range of materials, including MoS_2,[12,13,15] WSe_2,[18,19,21] and $MoTe_2$.[23−26] For top gating, ionic liquids have been widely used to facilitate charge control in MoS_2,[16,28−30] WSe_2,[22,31,32] and $MoTe_2$[27] FETs. Solid polymer electrolytes have also been used as top gate dielectrics and applied to, for example, carbon nanotubes,[33,34] graphene,[35,36] MoS_2,[37] and WSe_2.[38] There are no prior reports of solid polymer gating of $MoTe_2$ which is intended here as a reconfigurable doping approach for TFET development.

Bulk 2H-$MoTe_2$ is an indirect band gap material, with a band gap in the range of 0.6 to 1.0 eV.[1,39−41] In monolayer form, a transition to a direct band gap is expected.[6,41] In contrast to the widely studied MoS_2 and WSe_2 FETs, $MoTe_2$-based FETs have gained attention only recently.[23−27] Ambipolar behavior has been reported for multilayer $MoTe_2$ FETs with ON/OFF ratio less than 4 decades,[23,26] and unipolar p-type behavior has been observed with an ON/OFF ratio greater than 6 decades.[24] The reported mobility is in the range of 0.3–20 cm^2/(V s) for holes,[23−25,27] and 0.03–30 cm^2/(V s) for electrons,[23,27] comparable to other TMDs.[1]

While TMD-based FETs appear promising, doping technologies for TMDs are still in a primitive stage. Traditional doping methods, such as ion implantation, are not

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suitable for atomically thin TMDs. Substitutional doping of MoS_2 with selenium during chemical vapor deposition has been shown to modulate the optical band gap by more than 10%, but transport data is lacking.[42] Nontraditional doping strategies, such as molecular doping and electrostatic doping using electrolytes, are being developed for TMDs.[18,30,43,44] For example, molecular doping using K or NO_2 has been demonstrated in WSe_2, where the doping mechanism is charge transfer between the dopant molecules and WSe_2.[18] A similar strategy using an amine-rich polymer, polyethylenimine, in multilayer MoS_2 led to successful *n*-type doping.[43] Besides molecular doping, electrostatic doping using ionic liquids and polymer electrolytes is an attractive alternative doping method for TMDs, at least for early device exploration.[27−38,44] Recently, by using an external gate voltage to drive ions to the surface of a TMD, ambipolar operation was demonstrated in multilayer MoS_2 using the ionic liquid 1-butyl-1-methyl pyrrolidiniumtris-(pentafluoroethyl)trifluorophosphate $[P14]^+[FAP]^-$.[44] Owing to the high gate efficiency of the electric double layer (EDL) formed at the interface between the electrolyte and WS_2, large n- and p-doping levels up to 9×10^{13} and 3.5×10^{13} cm^{-2}, respectively, have been reported from Hall measurements.[44] The huge charge carrier densities that can be induced by electrolyte gating makes possible the experimental observation of spin splitting in WSe_2.[31] Ionic liquids have been used to create a p−n junction in MoS_2 at 180 K, where the location of the junction can be tuned by the magnitude of the applied source-drain voltage.[30] One advantage of solid polymer electrolytes compared to liquid electrolytes is that a top gate can be evaporated onto the electrolyte surface, and it has recently been shown that poly(ethylene oxide) (PEO) can be patterned using electron-beam lithography.[45]

In the absence of a robust doping technology, we have implemented an ion-doping method based on prior work in organic semiconductors and graphene.[35,36,46] This method is generally applicable to TMD devices and enables reconfigurable n- and p-type doping and the ability to establish p−n junctions. Doping is achieved using a solid polymer electrolyte, PEO and $CsClO_4$, on 2H-$MoTe_2$. Typically, sheet carrier densities on the order of 10^{13} to 10^{14} can be expected due to the large EDL capacitance, ranging from a few to tens of $\mu F/cm^2$.[2,35,36,46,47] Such high carrier densities are not easy to achieve in normal metal-oxide gate stacks, especially when the channel is based on layered, van der Waals materials, where a high quality oxide is difficult to deposit.[19,48] The thickness of the 2H-$MoTe_2$ in this study is ~6 nm (~9 monolayers). While lithium-based salts are appropriate in the extreme case of monolayer TMDs,[37,38] Li^+ can intercalate into multilayer TMDs, degrading the semiconducting property and potentially fracturing the channel due to volumetric changes.[49,50] Therefore, we choose a salt with a large cation, $CsClO_4$, to prevent intercalation.

In this paper, we show that the PEO:$CsClO_4$− gated $MoTe_2$ FET can be efficiently reconfigured between n- and p-channel operation with ON/OFF ratios of 10^5 and subthreshold swings of 90 mV/decade. The formation of an EDL at the interface of the polymer electrolyte and $MoTe_2$ enables us to estimate the band gap energy of few-layer $MoTe_2$ to be ~0.8 eV. The capacitance of the double layer is measured by a DC method to be ~4 $\mu F/cm^2$. The extracted field-effect mobilities are 7 and 26 $cm^2/(V\ s)$ for electrons and holes, respectively, while a maximum sheet carrier density of 1.6×10^{13} cm^{-2} is achieved. Finally, taking advantage of the feasibility of the reconfigurable doping, stable p−n junction doping is demonstrated at 220 K.

RESULTS AND DISCUSSION

Prior to applying the electrolyte gate, the transfer and output characteristics of the $MoTe_2$ were measured (Figure 1). A cross-sectional schematic of the back-gated 2H-$MoTe_2$ device is provided in Figure 1a. An AFM image of the device immediately after source/drain fabrication is illustrated in Figure 1b, and a line scan indicates a flake thickness of 5.6 nm, corresponding to 8 monolayers. The surface roughness of the SiO_2 and 2H-$MoTe_2$ are 0.3 and 0.4 nm, respectively. The channel width and length are 1.4 and 1 μm, respectively. The room temperature transfer characteristics of the device are shown in Figure 1c at various source-drain voltages (V_{DS}). The device shows ambipolar behavior with a minimum current at the back gate voltage (V_{BG}) of −25 V. When V_{BG} increases from −25 to 60 V, the drain current (I_D) increases by more than 3 decades, indicating electron accumulation in the channel. When V_{BG} decreases from −25 to −60 V, I_D becomes dominated by holes, as evidenced by increasing I_D. Within the applied V_{BG} range, the ON/OFF ratio of the hole branch is less than two decades, and the electron branch is slightly more than three decades. The output characteristics of the device are shown in Figure 1d, where I_D is a nonlinear function of V_{DS} for both electron and hold branches. This suggests that transport is Schottky-barrier limited in the $MoTe_2$ FET. This also explains the relatively small current at $|V_{DS}| = 2$ V, which is only 300 nA/μm for the electron branch at $V_{BG} = 60$ V and 4 nA/μm for the hole branch at $V_{BG} = -60$ V.

Ion-gating is achieved by depositing PEO:$CsClO_4$ and a metal top gate (TG) onto the same FET presented in Figure 1. The channel can be doped n- or p-type simply by applying voltages of opposite polarity to the top gate. As illustrated by the transistor schematic in Figure 2a, when a positive top gate voltage (V_{TG}) is applied, Cs^+ ions are driven to the surface of the channel, which induce electrons in the $MoTe_2$, doping it n-type. The positive ions and the induced electrons

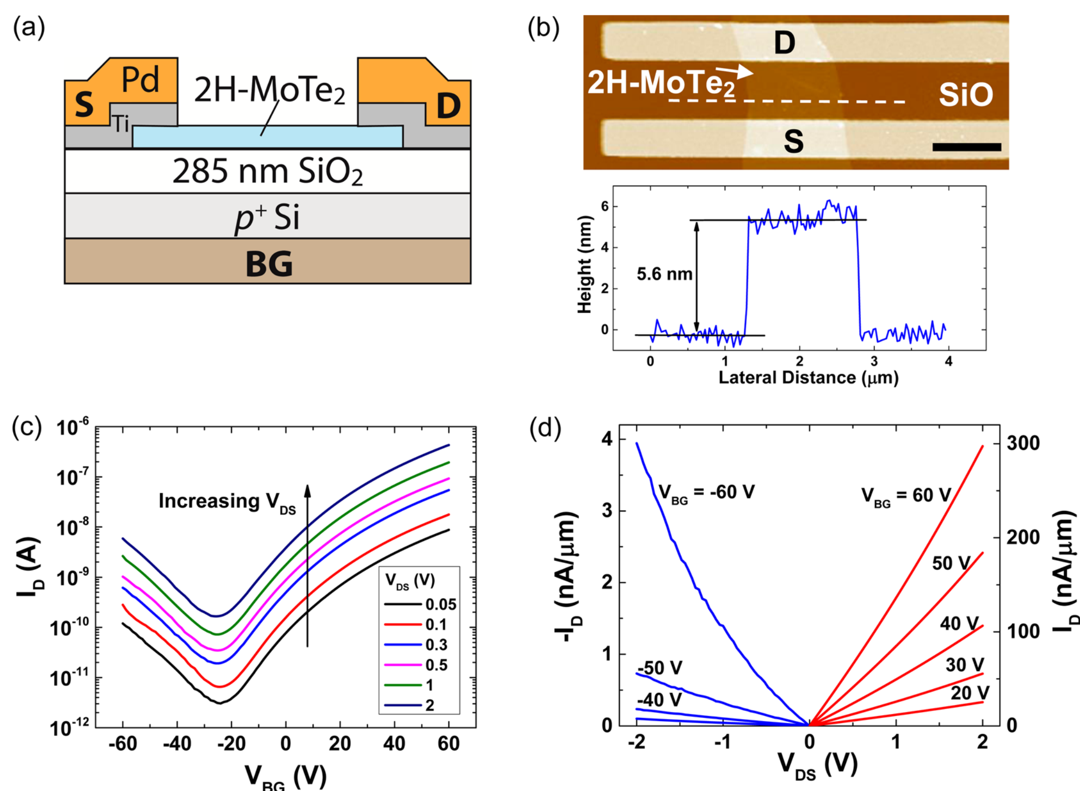

Figure 1. Room temperature current−voltage characteristics of a back-gated 2H-$MoTe_2$ field-effect transistor (FET). (a) Schematic cross section of the FET. (b) Top: AFM scan of the fabricated FET; scale bar, 1 μm. Bottom: AFM line scan corresponding to the white dashed line. (c) Transfer characteristics of the FET shown in (b) at various V_{DS}. (d) Common-source transistor characteristics of the electron (red curves) and hole (blue curves) conduction branches of the same device.

form an EDL, the thickness of which is typically ∼1 nm.[44,46,47] Similarly, a p-type channel can be realized by applying a negative V_{TG} where ClO_4^- ions dope the channel and induce holes. The doping level depends on the capacitance of the EDL and the magnitude of the applied V_{TG}.

The transfer characteristics of the ion-gated FET are illustrated in Figure 2b. The source and back gate terminals were grounded. Considering the low mobility of ions in PEO at room temperature,[51] we use a slow sweep rate of 1 mV/s when measuring the ion-gated device at room temperature to provide sufficient time for the ions to respond to the applied field. We determined that 1 mV/s is sufficiently slow by decreasing the sweep rate until the double sweep was essentially hysteresis-free (see Supporting Information). To eliminate any effects from previous measurements, all device terminals were grounded for 5 min between measurements, providing the ions sufficient time to return to equilibrium.

With ion-gating, the ON/OFF ratio increases from a few orders of magnitude to greater than 5 decades for both electron and hole branches. At V_{DS} = 0.05 V, the ON current is ∼1 μA for the electron branch at V_{TG} = 0.4 V, and 4 μA for the hole branch at V_{TG} = −1.6 V, while the OFF current is less than 10 pA. The subthreshold slopes (SS) are 100 and 87 mV/decade for the electron and hole branches, respectively. Multiple ion-gated devices were measured and all showed similar behavior. These SS swing values are smaller than those reported by Lezama and co-workers for an ionic liquid-gated $MoTe_2$ FET (140 mV/decade for electrons and 125 mV/decade for holes) and show significantly smaller hysteresis over a comparable voltage range and sweep rate.[27]

Compared to the back-gated device without the electrolyte (Figure 1), the ON current and the ON/OFF ratio in the ion-gated device are two decades larger for the electron branch and four decades larger for the hole branch at V_{DS} = 0.05 V. The strong current modulation with the top gate implies that the EDL was formed at the interface of the electrolyte and the $MoTe_2$ channel. Figure 2c,d shows the common source characteristics (I_D−V_{DS}) at various V_{TG} for the electron and hole branches, respectively. Drain current increases linearly with drain-source voltage and then gradually saturates. The saturation current is ∼3.6 μA/μm at V_{TG} = 0.4 V for the electron branch and 7 μA/μm at V_{TG}= −1.6 V for the hole branch. The I_D−V_{DS} relation is similar to the Si MOSFET, where current is limited by thermal emission over an energy barrier at the source end of the channel. This can be expected in the top-gated devices due to the small (∼1 nm) electrostatic length resulting from the ion doping.[33,44] The large induced sheet carrier density at the source/drain end increases the tunnel current in the Schottky barriers

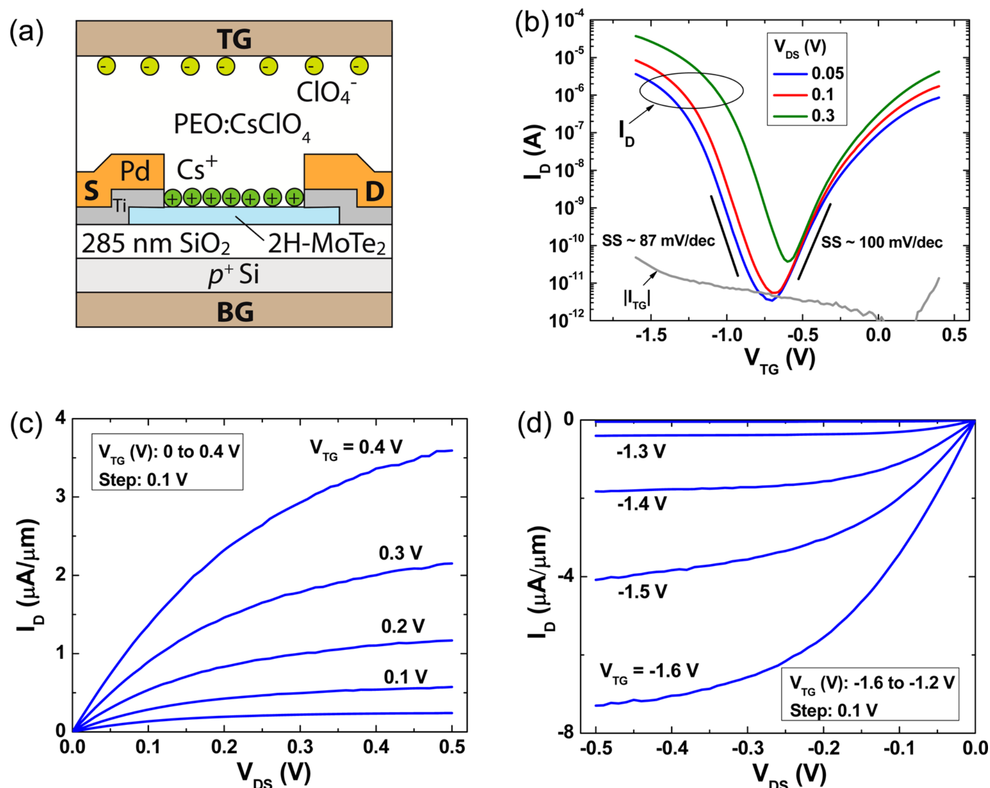

Figure 2. Room temperature current−voltage characteristics of a PEO:$CsClO_4$ solid polymer electrolyte-gated 2H-$MoTe_2$ FET. (a) Schematic device cross section. (b) FET transfer characteristics showing drain current *vs* top-gate voltage at various supply voltages. The gate leakage current (I_{TG}) is measured at the top gate. The two solid black lines show the subthreshold swings for the electron and hole branches, respectively. Common-source transistor characteristics are shown for the electron branch in (c) and the hole branch in (d).The back gate was grounded and the sweep rate was 1 mV/s.

resulting in nearly ohmic transport for both electrons and holes. Thus, transport inside the channel mainly limits the current in the top-gated $MoTe_2$ transistor. This is very different from the back-gated device of Figure 1, where the current is limited by thermionic emission through the Schottky barriers. To quantitatively capture the difference, it is instructive to compare the electrostatic length (λ) in the two systems, which describes the extension of the electric field lines from the source/drain contacts into the channel region.[52,53] In a planar structure, λ is quantified as $\lambda = (\varepsilon_{CH}\, t_{CH}\, t_{OX}/\varepsilon_{OX})^{1/2}$,[52,53] where ε_{CH} is 12 for the $MoTe_2$ channel,[54] and t_{CH} of the $MoTe_2$ is 5.6 nm as measured by AFM. For the electrostatic double layer the $t_{OX} = t_{EDL} \cong 1$ nm and $\varepsilon_{OX} = \varepsilon_{EDL} = 5$.[33,51] On formation of the EDL using the top gate, $\lambda = 3.7$ nm; however, using the electrostatic doping from the back-gated FET, $\lambda = 62$ nm, with $\varepsilon_{OX} = 3.9$ and $t_{OX} = 285$ nm; this is more than 18 times larger than in the top-gated FET. As a result, we may expect thick Schottky barriers in the back-gated $MoTe_2$ transistors with 285 nm SiO_2, and thin barriers for easier electron tunneling in the top-gate devices with an EDL.

We also highlight the distinct difference between the transfer characteristics of the two systems in the subthreshold region of the electron branch. At the same positive V_{DS} values of 0.05, 0.1, and 0.3 V, the drain currents for the top-gated FET overlap in the subthreshold region (Figure 2b), while I_D increases exponentially as a function of V_{DS} in the back-gated device (Figure 1b). This difference may also be explained by the different transport mechanisms in the two devices. In the top-gated case, because the channel length of 1 μm is much larger than the natural length ($\lambda \sim 3$ nm), short-channel effects can be excluded, and thus the overlap is expected for V_{DS} larger than a few k_BT/q (∼26 mV at room temperature),[55] where k_B is Boltzmann constant and T is absolute temperature. However, in the back-gated case, the current is mainly limited by back-to-back Schottky barriers, where V_{DS} mainly drops at the barriers instead of the channel region. When V_{DS} increases from 0.05 to 2 V, as shown in Figure 1c, the Schottky barrier height at the drain end becomes lower, and the Schottky barrier at the source end becomes thinner. Thus, larger I_D is expected with larger V_{DS} whether the device is in the subthreshold region or the ON region.

The strong ambipolar behavior shown in Figure 2b suggests that the Fermi level in the energy band diagram was shifted from the valence band edge to the conduction band edge when the gate voltage was swept from −1.6 to 0.4 V. The I_D−V_{TG} curve in Figure 2b is shown on a linear scale in Figure 3a. The V_{TG} of the OFF state ranges from −1.1 to −0.1 V, indicating the

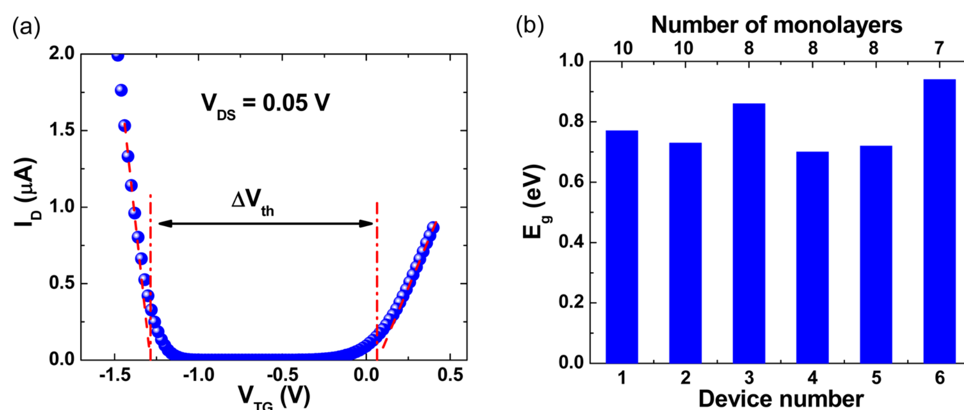

Figure 3. Quantitative determination of the band gap (E_g) of 2H-$MoTe_2$. (a) Linear scale plot of the I_D-V_{TG} transfer curve as shown in Figure 2b. The intersection points of the red dashed lines with the *x* axis indicate the threshold voltages, $V_{th,p}$ and $V_{th,n}$, of the hole and electron branches, respectively. (b) Computed band gap for six devices, with an average of 0.8 eV. The band gap for each device was calculated based on ΔV_{th} in (a).

band gap of the channel material. Following previous studies,[34,44] we estimate the band gap energy (E_g) of the 2H-$MoTe_2$ using the empirical formula $E_g = \alpha q \Delta V_{th}$.[34] Here, q is the electronic charge and $\Delta V_{th} = \Delta V_{th,n} - \Delta V_{th,p}$, where $V_{th,n}$ and $V_{th,p}$ are the threshold voltages of the electron and hole branches, respectively. These values are highlighted by the dashed lines in Figure 3a. The parameter α is defined as $\alpha = SS_{60}/SS_M$, where SS_{60} is the subthreshold slope at the thermal limit (60 mV/decade at room temperature), SS_M is the measured subthreshold slope of the device. A SS_M of 94 mV/decade is extracted from the transfer characteristics in Figure 2b by averaging the electron and hole subthreshold swings, giving an α value of ~0.64. With $\Delta V_{th} = 1.35$ V extracted from Figure 3a, this yields $E_g \sim 0.86$ eV at room temperature. The E_g values for six devices are shown in Figure 3b. The $MoTe_2$ flake thicknesses of devices 1 to 6 are 7.0, 7.0, 5.6, 5.6, 5.6, and 5.0 nm, respectively (devices 3, 4, and 5 were fabricated on the same flake), corresponding to 10, 10, 8, 8, 8, and 7 monolayers. The extracted E_g ranges from 0.70 to 0.94 eV with an average of 0.8 eV, and this result agrees well with previous theoretical studies,[6,39−41] and a recent experimental report of $MoTe_2$ gated with an ionic liquid.[27] It has been reported that E_g increases weakly within 4−6 monolayers, and increases strongly below 3 monolayers (*i.e.*, ≤ 2 nm).[11,56,57] Considering our flake thickness, we expect the E_g reported here to be similar to that of the bulk $MoTe_2$ crystal. We noticed that E_g extracted from the device fabricated on a 5 nm thick $MoTe_2$ flake (7 monolayers) is 0.94 eV, which is slightly larger than those extracted from devices with 6 or 7 nm thick flakes. This may be a result of the quantum confinement effect; however, considering the fluctuations in E_g for devices built with flakes of similar thickness, more devices must be measured to confirm this conclusion.

As discussed above, one of the advantages of ion-gating is the strong gate coupling due to the large C_{EDL}, which can range from a few to tens of $\mu F/cm^2$. Here we determine C_{EDL} with a DC measurement. A map of I_D for various V_{TG} and V_{BG} is plotted on a logarithmic scale in Figure 4a. The data were measured by fixing V_{BG} at one value while sweeping V_{TG} with V_{DS} fixed at 0.05 V. For a given V_{BG}, the electron and hole conduction branches appear at the right and left sides of the conduction minimum respectively, where the minimum is indicated by the dark regions. The location of the minima in V_{TG} is a function of V_{BG}. Specifically, the conduction minimum shifts to more negative V_{TG} values as the V_{BG} becomes more positive. The extent of the shift along the V_{TG} axis is almost linearly proportional to the V_{BG} applied, as shown in the bottom plot of Figure 4a for different current levels for electron and hole branches. The triangles and the squares are experimental data and the solid lines represent a linear fit to each set of experimental data with the same current. The slopes of the solid lines (*i.e.*, $\Delta V_{BG}/\Delta V_{TG}$) are 370, 360, 305, and 316 from the left green curve to the right blue curve, giving an average of 338. For the double-gated device with a thin channel and thick back gate oxide, this ratio can be used to calculate the capacitance of the electric double layer (C_{EDL}) as $C_{EDL}/C_{OX} = -\Delta V_{BG}/\Delta V_{TG}$.[58,59] Using $\varepsilon_{OX} = 3.9$ and $t_{OX} = 285$ nm, C_{OX} is 0.0121 $\mu F/cm^2$, giving C_{EDL} of ~4 $\mu F/cm^2$. Using the parallel-plate capacitor model and assuming the relative dielectric constant of the electrolyte is 5,[51] the thickness of the EDL (t_{EDL}) is estimated as 1 nm. The extracted C_{EDL} and t_{EDL} agrees well with previous studies.[33,35,47]

The C_{EDL} and the transfer characteristics can be used to extract the field-effect mobility, μ_{FE}, above threshold $\mu_{FE} = (1/C_{EDL})\partial\sigma/\partial V_{TG}$,[24] where σ is the conductivity of the channel, defined as $\sigma = (L/W)\, I_D/V_{DS}$ and L and W are the length and width of the channel, respectively. The dependence of σ on V_{TG} is shown in the inset of Figure 4b, and the extracted μ_{EF} is shown in the main panel. The maximum μ_{FE} is 7 $cm^2/(V\,s)$ for electrons and

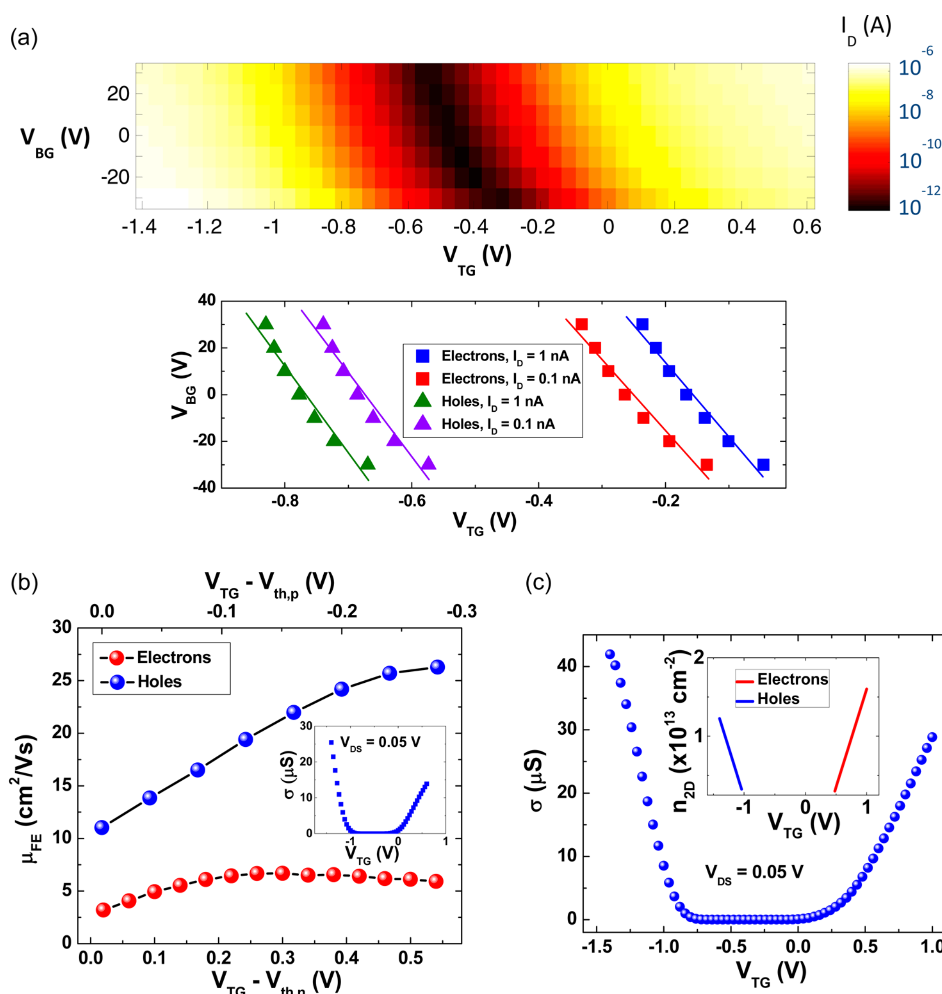

Figure 4. Quantitative determination of the electric double layer (EDL) capacitance, $MoTe_2$ channel field-effect mobility, and sheet carrier density. (a) Top: Drain current map at various top gate and back gate voltage plotted on a logarithmic scale for a supply voltage of 0.05 V and a sweep rate of 1.3 mV/s. Bottom: Linear fit (solid lines) of the experimental data (squares and triangles) at fixed drain current. (b) Field-effect mobility as a function of top gate voltage above threshold for electrons (red spheres) and holes (blue spheres) respectively. Inset: Channel conductivity as a function of top gate voltage measured at V_{DS} = 0.05 V and V_{BG} = 0. (c) Conductivity as a function of top gate voltage for another FET measured over a larger top gate voltage range. The inset shows the estimated sheet density as a function of top gate voltage for electrons (red curve) and holes (blue curve) above threshold.

26 cm^2/(V s) for holes, similar to a recent study on few-layered 2H-$MoTe_2$ transistors gated with thermal SiO_2[24] and an ionic liquid.[27]

Figure 4c shows σ measured in another device with a relatively larger V_{TG} range from −1.4 to 1.0 V. Channel conductivity increases with $|V_{TG}|$ and reaches 29 μS at V_{TG} = 1.0 V for the electron branch and 42 μS at V_{TG} = −1.4 V for the hole branch. Assuming a constant C_{EDL} throughout the entire V_{TG} range, the sheet charge carrier density (n_{2D}) in the channel well above the threshold voltage may be estimated as, $n_{2D} = C_{EDL}|V_{TG} - V_{th}|/q$.[60] As reported in the inset of Figure 4c, the maximum doping level of the electron branch is 1.6 × 10^{13} cm^{-2} at V_{TG} = 1.0 V, and the hole branch is 1.2 × 10^{13} cm^{-2} at V_{TG} = −1.4 V.

The ion-gating technique makes it feasible to build 2D devices with different doping polarity and doping levels; however, as shown above, both the doping polarity and level depend on the applied external voltages and are sensitive to the top gate, drain/source, and back gate voltages. Moreover, slow sweep rates are required to drift the ions into place. What is needed is the ability to drive the ions to the surface of the $MoTe_2$ using an applied field, and "lock" them into place at the surface so that fast voltage sweep rates can be used to measure the drain current. This can be achieved by driving the ions to the surface of the $MoTe_2$ and quenching the device to a temperature lower than the glass transition temperature (T_g) of the solid polymer electrolyte (see Supporting Information, Figure S2). When temperature is less than T_g, the polymer chains are kinetically arrested and the polymer relaxation times become large. Because ion mobility is strongly coupled to polymer mobility, the ionic conductivity through the polymer becomes negligibly small (∼10^{-12} S/cm).[61] Consequently, the EDL is locked

into position at the $MoTe_2$ interface, and the doping polarity and doping level become fixed and are no longer controlled by the top gate. However, top gate control is recovered after the sample is heated to room temperature, and the transfer characteristics become identical to those prior to quenching, demonstrating that no irreversible changes occurred to the device (see Supporting Information, Figure S5).

In addition to unipolar doping where either cations or anions are driven to the surface of $MoTe_2$, we use this technique to create p−n junction doping where both cations and anions are driven to the surface.[30] The specific case of the p−n junction doping is illustrated by the process flow in Figure 5a (A−D). In this device, we replaced the thick SiO_2 dielectric used above with 27 nm of Al_2O_3 grown by atomic layer deposition (ALD), because the thinner high-k dielectric offers better gate control over the channel. Also, the two-contact devices presented above were replaced with a four-terminal contact structure to allow the contact resistance to be extracted.

Both unipolar doping and p−n junction doping can be simultaneously achieved in separate regions of the device by the selection of terminal biases. Schematic A shows a four-contact device covered by PEO:$CsClO_4$ under thermal equilibrium at room temperature. No external voltage is applied and the ions are homogeneously distributed. Here, instead of using the top-gate bias to drive the ions, we can uniformly bias the top 4-terminals with respect to the back gate for unipolar doping or ground the back gate and apply a drain/source bias to form a p−n junction. In Schematic B, terminals 2 and 3 are biased at room temperature with positive voltage (+V) and negative voltage (−V) respectively, the back gate is grounded, and terminals 1 and 4 are floated. Under these bias conditions, negative ions will accumulate near terminal 2 and positive ions near terminal 3. As a result, the channel region close to terminal 2 becomes p-type doped while the channel region close to terminal 3 becomes n-type doped. A p−n junction is expected between terminals 2 and 3. In Schematic C, the device is quenched to 220 K, which is 24 K below the T_g of the polymer. The bias condition in Schematic B is maintained during quenching until 220 K is reached.

An AFM image of the four-terminal device on Al_2O_3/Si is shown in Figure 5a-D, where the flake thickness is 6 nm and the channel width is ∼3.8 μm. The distance between terminals 1 and 4 is 2 μm, and terminals 2 and 3 are positioned such that the channel is divided into three regions of equivalent length (∼0.6 μm). Before depositing the electrolyte, we measured the room temperature I−V and extracted a source resistance of 5.5 k$\Omega\cdot\mu$m using the four-probe method (see the Supporting Information for details). The source resistance is the contact resistance plus the series resistance originating from the interlayer transport.[62]

The device characteristics for the condition corresponding to Schematic A (*i.e.*, homogeneous ion distribution with no applied bias) are shown in Figure 5b. Here, the device temperature has been reduced to 220 K. The drain-to-source voltage was applied between terminals 1 and 4, with terminals 2 and 3 floating. The device shows ambipolar behavior with a linear I_D−V_{DS} relationship at low V_{DS} and saturating behavior at large V_{DS} for both electron and hole branches. The ON current is about 0.6 μA/μm for both electron and hole branches at V_{BG} of 4 and −6 V, respectively. The inset shows the transfer characteristic of the same device with electron and hole branches distributed almost symmetrically around V_{BG} of −1 V. These data suggest that the Fermi level lies close to the middle of the energy band gap at a back-gate bias of approximately −1 V.

The device characteristics obtained after the doping and quenching process described in Figure 5a are illustrated in Figure 5c. Here, 1.5 and −1.5 V are applied to terminals 2 and 3 during the quenching process, yielding p-type doping in the channel between terminals 1 and 2, and n-type doping between terminals 3 and 4 (Schematics B and C). The ON current in both n- and p-type channels exceeds 50 μA/μm, and the conductivity is more than two decades larger than the device without ion doping at a similar back gate voltage.

I_D as a function of V_{DS} in Figure 5d shows the I−V characteristics of the four top-surface terminals for four combinations of terminals. The carrier transport from terminal 2 to 3 shows rectifying behavior, indicating a p−n junction in the channel between terminals 2 and 3 as anticipated from Figure 5a, Schematic C. The same behavior is also measured when V_{DS} was biased between the two most outer terminals, 1 and 4, as would be expected. Contact pairs 1−2, and 3−4 are ohmic because the ion doping increases the tunneling transparency of the Schottky contacts. The rectifying behavior shown in Figure 5d is therefore due to the formation of a p−n junction and not due to a Schottky barrier.

To simplify further discussion, we label the device with V_{DS} biased at terminals 1 and 4 as diode A, and the one with V_{DS} biased at terminals 2 and 3 as diode B. Figure 5e shows the I_D *versus* V_{DS} on a logarithmic scale for diodes A and B. The forward bias current increases rapidly with V_{DS}, giving a slope of 100 mV/decade when V_{DS} increases from 0.4 to 0.7 V. The theoretical limit for a diode limited by thermal transport is ln(10) k_BT/q. This yields 44 mV/decade at 220 K. The p−n junction current in bulk semiconductors is given by $I = I_0[\exp(qV/\eta k_BT) - 1]$,[55] where, I_0 is the reverse saturation current and η is the diode ideality factor. For $\eta = 1$, the current is diffusion current dominated, while for $\eta = 2$, the current is limited by recombination.[55] In our device, η is ∼2.3, suggesting that

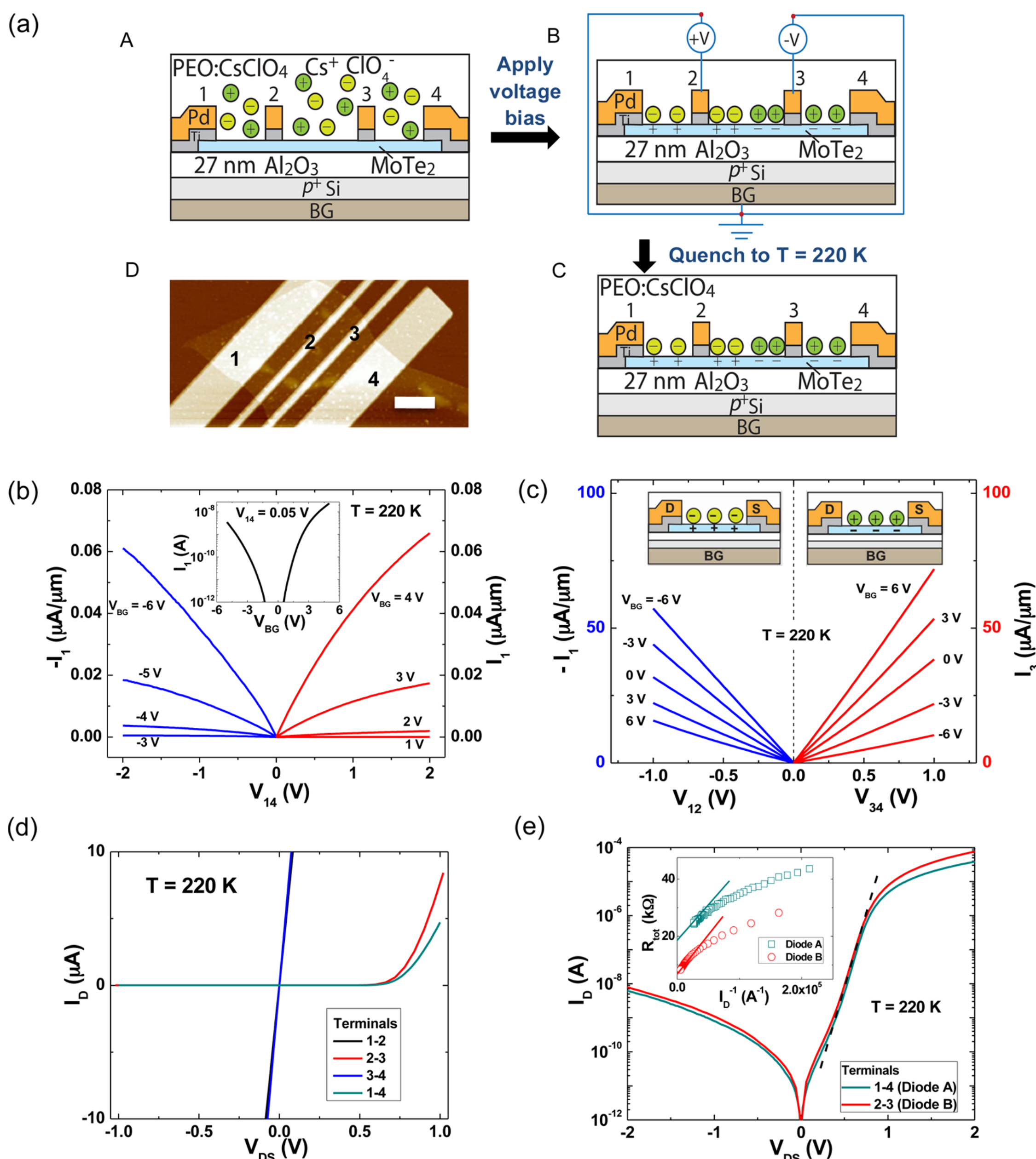

Figure 5. Unipolar doping and p−n junction formation using PEO:$CsClO_4$ solid polymer electrolyte at 220 K. (a) Mechanism for p−n junction formation. (A) In thermodynamic equilibrium the ions are homogeneously distributed. (B) Terminals 2 and 3 are connected to sources that set plus and minus DC voltages with respect to the back gate, with terminals 1 and 4 floating. Ions redistribute in the electric fields of the contacts to reach the steady state configuration shown. (C) The ions are locked into place by quenching the device to 220 K. (D) AFM scan of the device before depositing PEO:$CsClO_4$. Scale bar: 1 μm. (b) Common-source characteristics measured at 220 K without ion gating (*i.e.*, by locking in the homogeneous distribution as shown in (a), Schematic A. Inset: the corresponding transfer characteristics. (c) Common-source characteristics measured between terminals 1 and 2 and between 3 and 4 with the other terminals floating. (d) Current−voltage characteristics on the indicated terminal pairs with the unconnected pairs floating, note that 1−2 and 3−4 are ohmic. (e) Semilog plot of the p−n junction *I*−*V* characteristic. V_{DS} was applied between terminals 2 to 3 and 1 to 4, respectively. The dashed line indicates the ideality factor. Inset: Total differential resistance (R_{tot}) as a function of I_D^{-1}. The *y*-axis intercept indicated by the solid lines suggests the series resistance of the diode.

recombination is significant in the $MoTe_2$ p−n junction. The forward bias current is about 40 and 80 μA at V_{DS} of 2 V for diodes A and B, respectively. The reverse current increases gradually with $|V_{DS}|$ and reaches ∼2.6 nA/μm at $V_{DS} = -2$ V, which is significantly larger compared to previous reports for monolayer WSe_2 (less than 0.05 nA/μm at the same V_{DS} of −2 V).[10] This may be partially due to the smaller band gap of $MoTe_2$ compared to monolayer WSe_2. Pronounced roll-off of I_D was observed when V_{DS} increases beyond 0.8 V due to the series resistance in the diode. Several methods can be used to extract the series resistance.[63] Here, we use the Werner method,[63,64] where, at large forward bias condition ($I \gg I_0$), the

$I-V$ relation for a diode including series resistance (R_S) $I = I_0[\exp[q(V - IR_S)/\eta k_B T] - 1]$ can be rewritten as $R_{tot} = k_B T/q\eta I^{-1} + R_S$. Here, R_{tot} is the differential resistance of a diode defined as R_{tot} = dV/dI, V is the drive voltage applied across the diode and I is the current of the diode. The y-axis intercept of the $R_{tot}-I^{-1}$ plot (inset of Figure 5e) suggests R_S, which is 18 and 7 kΩ for diodes A and B, respectively.

CONCLUSION

In summary, an electrostatic gating method using a solid polymer electrolyte, PEO:$CsClO_4$, on 2H-$MoTe_2$ is demonstrated for the first time. The electrolyte enables efficient reconfiguration of the device between n-channel and p-channel operation with n- and p-doping levels up to 1.6×10^{13} and 1.2×10^{13} cm^{-2} at room temperature. Such high doping levels are promising for the future demonstration of tunnel field-effect transistors (TFETs), and the study of spin-splitting and superconducting TMDs. The band gap energy of $MoTe_2$ (7−10 monolayers) is quantitatively estimated to be ~0.8 eV, in good agreement with theoretical predictions. The field-effective mobility is extracted as 7 and 26 cm^2/(V s) for electrons and holes at room temperature, respectively, which is comparable to other TMDs such as MoS_2 and WSe_2. By quenching the device to 220 K, stable unipolar and p−n junction doping is realized. The ideality factor of the junction is 2.3, suggesting that the p−n junction is recombination dominated.

METHODS

2H-$MoTe_2$ was mechanically exfoliated from either powder or crystal using the Scotch tape method. $MoTe_2$ from powdered exfoliation (99.9% American Elements) was used to construct the 2-terminal devices, while $MoTe_2$ exfoliated from the bulk crystal (2d Semiconductors, Inc.) was used for the 4-terminal devices. The flakes were transferred onto a highly p-doped Si substrate with 285 nm of thermal SiO_2. The flake thickness, measured by atomic force microscopy (AFM), ranged from 5−7 nm, or 7−10 monolayers assuming a monolayer thickness of 0.7 nm.[39] Source and drain contacts of Ti (1 nm)/Pd (60 nm) were deposited by electron-beam lithography and electron-beam evaporation, followed by lift-off in acetone at room temperature.

To prepare the ion gate, PEO (molecular weight 95 000 g/mol, Polymer Standards Service) and $CsClO_4$ (99.999%, Sigma-Aldrich) were dissolved in anhydrous acetonitrile (Sigma-Aldrich) with a solution concentration of 1 wt % and a PEO ether oxygen to Cs^+ molar ratio of 76:1. The solution was drop-cast onto the back-gated $MoTe_2$ devices under ambient conditions, followed by a 3 min anneal at 90 °C on a hot plate in air. The thickness of the cast electrolyte was ~1 μm, measured by AFM. To prepare the top metal gate, 50 nm of Pd was evaporated onto the solid PEO:$CsClO_4$ film using a shadow mask and electron-beam evaporation. An optical image of the top-gated device is provided in the Supporting Information.

Electrical characterization was performed using a Cascade Microtech PLC50 Cryogenic vacuum probe station at ~10^{-5} Torr. Because PEO-based electrolytes can absorb as much as 10 wt % water under ambient conditions,[65] the sample was annealed under vacuum at 350 K for 3 min. To facilitate the removal of water by increasing the polymer mobility, the annealing temperature was chosen to be ~20 degrees larger than the melting temperature (T_m) of the PEO:$CsClO_4$. The T_m (58 °C) and T_g (−29 °C) of the polymer electrolyte were measured by differential scanning calorimetry, and the data are provided in the Supporting Information. After annealing, the heater was turned off and the temperature decreased to room temperature over 4 h.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Optical image of the top-gated device; DSC measurement of PEO:$CsClO_4$ melting and glass transition temperatures; transfer characteristics of the top-gated device at varying sweep rate; room temperature electrical characteristics of the back-gated FET; transfer characteristics of the electrolyte-gated FET before and after quenching. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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